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High-Efficiency Error Amplifier Design in 0.35μm CMOS Technology

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Abstract: Error amplifiers are extensively employed in integrated circuits, necessitating the design of high-performance variants. This study utilizes a 0.35μm CMOS process to develop a high-performance error amplifier, with a theoretical analysis of its performance. Cadence simulations indicate that the error amplifier designed in this study achieves a common mode input range of 66mV to 2.8V, a settling time of 268ns, and a slew rate of 5.4V/μs.

Keywords: Error Amplifier, ICMR, Settling Time, Slew Rate.

1. Introduction

Error amplifiers [1-3] are the most commonly used in integrated chips, which can realize the functions of high input impedance and low output impedance, and have the functions of short and short, which are widely used in analog circuits such as DC-DC and LDO, as well as in analoghybrid circuits such as ADC.

2. Operating Principle of High Performance Error Amplifier

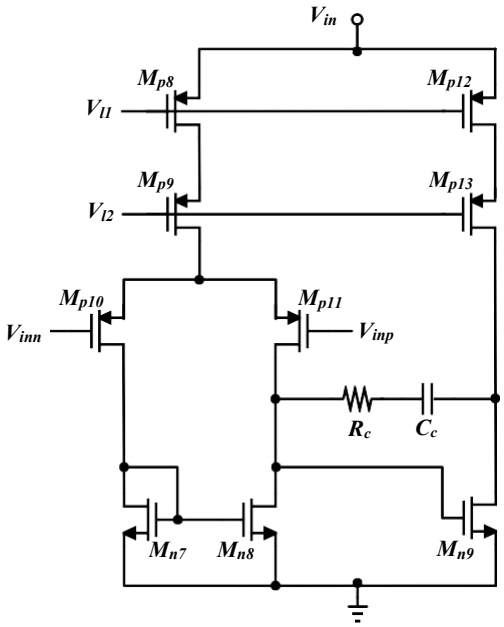

Figure 1. Schematic diagram of high performance error amplifier

As shown in Figure 1, the error amplifier in the band-gap reference voltage source is composedof M_{p8}~M_{p13}, M_{n7}~M_{n9}, R_c and C_c. It adopts a two-stage structure, and the second stage is the

cascode current source as the load common source output stage, so as to improve the open- loop gain of the error amplifier and further improve the power supply interference suppression ability of BGR. Because the two-stage structure amplifier is not stable, Miller compensation circuit is introduced, that is, Miller compensation [4, 5] capacitor C_c and zero resistance Rc are added. The stability of the error amplifier is analyzed by using ac small signal modeling. The equivalent model of the error amplifier is shown in Figure 2:

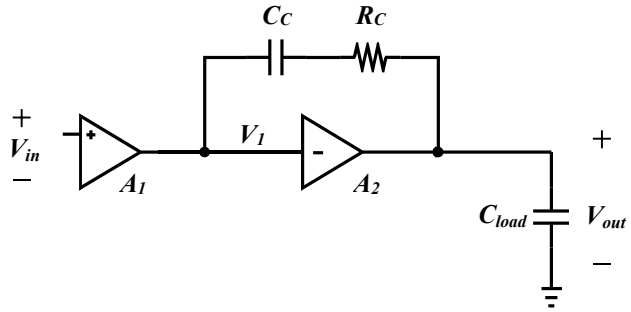

Figure 2. Equivalent model of error amplifier

Modeling of AC small signal in Figure 2 is shown in Figure 3:

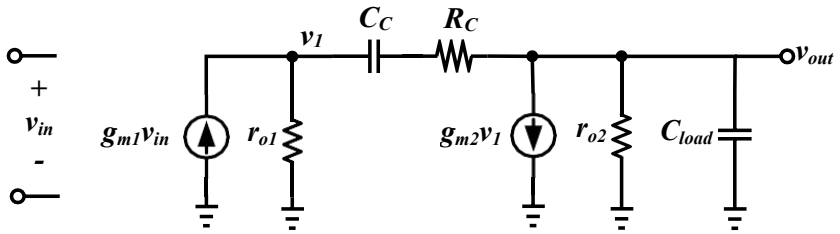

Figure 3. AC small signal model of error amplifier

Where, G_{M1} and R_{O1} are the equivalent transconductance and output impedance of the first differential input stage of the error amplifier, and G_{M2} and R_{O2} are the equivalent transconductance and output impedance of the second common source amplifier.

3. Numerical Experiments

3.1. Analysis and simulation of DC characteristics

The common mode voltage input range (ICMR) of the error amplifier is the range of common mode voltage of the differential input to the tube that is allowed when the circuit is in normal operation. It can be seen from Figure 4 that the common mode input range of the error amplifier designed in this paper is 66mV~2.8V.

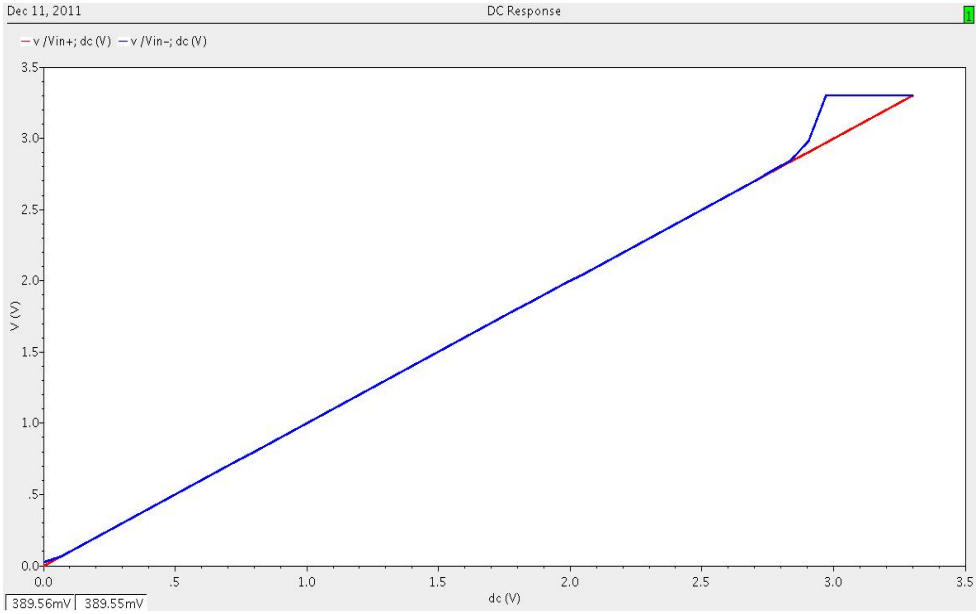

Figure 4. Common mode voltage input range

3.2. Analysis and simulation of transient (TRAN) characteristics

Simply setting up the error amplifier with an expression Time is a structure that attaches it to the buffer with a step signal of 10ns in range and 1V in range at the same end of the error amplifier, for the Time it takes for the output voltage to jump in and then simply settle on the output. According to Figure 5, the establishment time of the error amplifier designed in this paper is 268ns, and the slew rate is 5.4V/ s.

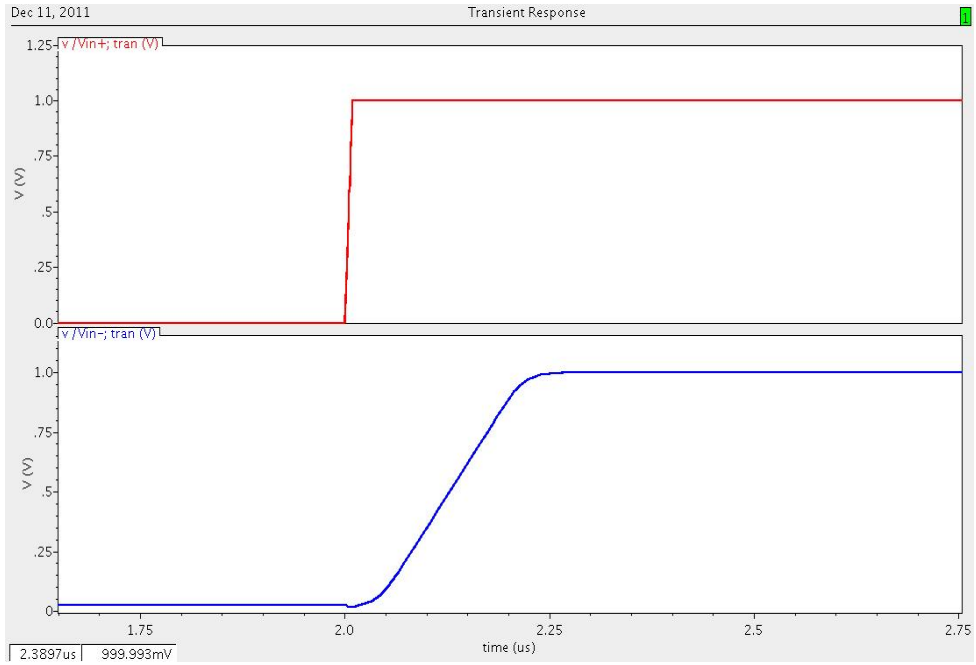

Figure 5. Setup time of error amplifier

4. Conclusion

A circuit structure of high performance error amplifier is designed and its theoretical derivation is carried out. Using 0.35 m CMOS process was designed, and the simulation results of the performance of the error amplifier were given.

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